(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 301 003 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
09.04.2003 Bulletin 2003/15

(51) Int Cl.[7]: **H04L 27/26**, H04L 1/06, H04B 7/08

(21) Application number: **02021726.1**

(22) Date of filing: **25.09.2002**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.09.2001 JP 2001303406**

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(54) Diversity Receiver unit for receiving an ofdm signal

(57) Respective demodulation modules (DMM1, DMM2) having AGC circuits (15, 16) include S/N detection circuits (29, 31), respectively, configured to detect their reception quality. The detection signals (sig1, sig2) of the S/N detection circuits (33) is supplied to a decision circuit (33) where their reception qualities are decided. In accordance with results of decision, a composition circuit (34) composes received data in such a ratio as to set better quality data as prevailing. data and eliminates any adverse effect on a diversity operation resulting from deteriorated quality data involved.

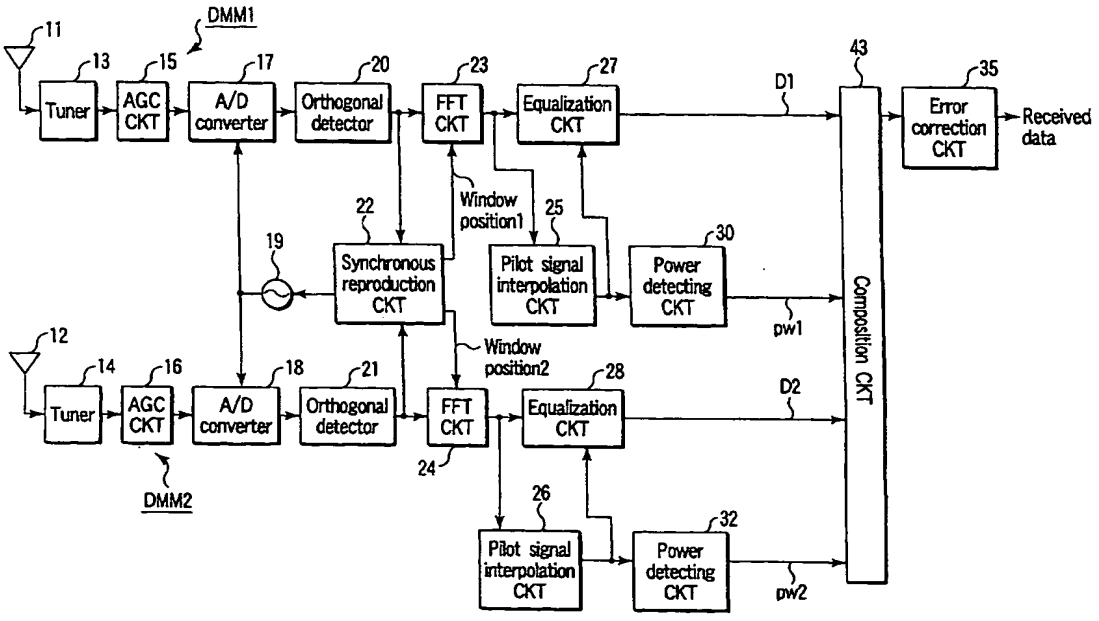

FIG. 1

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Description

[0001] This invention relates to a receiver unit applied to, for example, an Orthogonal Frequency Division Multiplex (hereinafter referred to as an OFDM) modulation system and, in particular, an OFDM receiver unit of a diversity configuration.

[0002] In recent years, attention has been paid to an OFDM modulation system as a modulation system for territorial digital broadcasting and mobile communication. It is known that, in mobile communications, etc., reception is affected by a fading phenomenon, and that reception performance can be improved in a radio unit of a diversity configuration having a plurality of demodulation modules. This type of receiver unit improves the reception performance by complementing a signal in a demodulation module of less reception power which results from a variation with a signal in another module of less variation.

[0003] FIG. 1 shows one example of a conventional OFDM receiver unit using the diversity configuration. This OFDM receiver unit has two demodulation modules, DMM1 and DMM2, both of the same structure.

[0004] Signals received from antennas 11 and 12 are supplied to tuners 13 and 14 in the demodulation modules, respectively. In these tuners 13 and 14, the frequency of the respective input signal is converted to an intermediate frequency (IF) band. The output signals of the tuners 13 and 14 are supplied to automatic gain control (AGC) circuits 15 and 16, respectively. The AGC circuits, even if receiving varying level input signals, effect control such that the output signal levels are constant. The output signals of the AGC circuits 15 and 16 are supplied to A/D converters 17 and 18, respectively. These A/D converters 17 and 18 convert the input signals to digital signals in accordance with a clock signal supplied from a later-described local oscillator 19. The output signals of the A/D converters 17 and 18 are supplied to orthogonal detectors 20 and 21 where they are converted to complex basebands signals. The output signals of the orthogonal detectors are supplied to a synchronous reproduction circuit 22 and to fast Fourier transformation (FFT) circuits 23 and 24.

[0005] The synchronous reproduction circuit 22 performs clock reproducing control and FFT window position control with the use of a method, etc., of finding, for example, a correlation between an effective symbol period and a guard period of the OFDM reception signal. For this reason, the synchronous reproduction circuit 22 outputs a clock control signal and window position control signal 2.

[0006] In the clock reproducing control, the clock control signal from the synchronous reproduction circuit 22 is supplied to the local oscillator 19 and controls the local oscillator 19 so that a difference between the clock signals is made smaller. The output signal from the local oscillator 19 is supplied to the A/D converters 17 and 18. For this reason, both demodulating modules are operated by a common clock signal.

[0007] Further, the FFT circuits 23 and 24 demodulate a subcarrier signal of the OFDM signal. This subcarrier signal contains a data signal and pilot signal. In the FFT window position control, the window position signals 1 and 2 outputted from the synchronous reproduction circuit 22 are supplied as window position indicating signals to the FFT circuits 23 and 24. These window position signals 1 and 2 are used as a start timing for FFT processing (transformation from a time domain to a frequency domain). The window position signals 1 and 2 can be independently set to the FFT circuits 23 and 24. The FFT circuits 23 and 24 are designed to accommodate a difference in the start timing. For this reason, the demodulation data from the FFT circuits 23 and 24 are outputted from the FFT circuits 23 and 24 at all times in the same timing.

[0008] The output signal from the FFT circuit 23 is supplied to a pilot interpolation circuit 25 and to an equalization circuit 27. The output signal from the FFT circuit 24 is supplied to a pilot interpolation circuit 26 and to an equalization circuit 28. The respective pilot interpolation circuits 25 and 26 interpolate a pilot signal inserted in a defined position of the OFDM signal. The interpolated pilot signal reveals a transmission path characteristic. The respective equalization circuits 27 and 28 generate a demodulation signal (subcarrier signal) as an output by performing a complex division calculation on the pilot signal and demodulation data supplied from the FFT circuits 23 and 24. The modulation signal has its distortion corrected and is brought back to a mapping position of the signal of its own.

[0009] Further, the interpolated pilot signals which are outputted from the pilot interpolation circuits 25 and 26 are supplied to power detection circuits 30 and 32, respectively, where calculation is made on the powers of the pilot signals. The signal powers from the power detection circuits 30 and 32, together with the output signals from the equalization circuits 27 and 28, are supplied to a composition circuit 43.

[0010] FIG. 2 shows one form of the composition circuit 43. In FIG. 2, the power values (pw1, pw2) of the pilot signals from the power detection circuits 30 and 32 are supplied to a proportion calculation section 431 where the following proportion values are calculated based on the power values pw1 and pw2 of the pilot signals.

$$f1 = pw1/(pw1 + pw2)$$

$$f2 = pw2/(pw1 + pw2)$$

[0011] The proportion value f1 is supplied to one input terminal of a multiplier 432 while, on the other hand, the proportion value f2 is supplied to one input terminal of a multiplier 433. A data signal D1 from the equalization

circuit 27 in the demodulation module DMM1 is supplied to the other input terminal of the multiplier 432 and a data signal D2 from the equalization circuit 28 in the demodulation module DMM2 is supplied to the other input terminal of the multiplier 433. In these multipliers 432 and 433, the data signals D1 and D2 are weighted by the proportion values f1 and f2.

[0012] The output signals of the multipliers 432 and 433 are supplied to an adder 434 where these signals are added together. The data signals from the respective demodulation modules are composed in this series of processing. Suppose that, for example, the power value pw1 of the pilot signal is "1" and pw2 is "0". Then the proportion value f1 from the proportion calculation section 431 becomes "1" and f2 becomes "0". Therefore, the output signal of the multiplier 432 is delivered as composite data from the adder 434.

[0013] The composite signal is supplied to an error correction circuit 35 shown in FIG. 1 and, as a final output, received data is outputted from the error correction circuit 35.

[0014] As set out above, in mobile communications, a received signal is strongly affected by the fading phenomenon and a received power greatly varies. If the received power becomes lower due to this variation, the reliability of demodulated data is lowered and there is a higher possibility of errors. These errors cause a deterioration in reception performance.

[0015] As shown in the composition circuit 43, therefore, calculation is made on the ratio of the signal power values outputted from the power detection circuits 30 and 32 and weight addition is so made as to be less affected by the reception data which is outputted from the demodulation module of a smaller reception power. By doing so it is possible to improve the reception performance.

[0016] It is necessary to consider the fact that the AGC circuits 15 and 16 are provided to the input stages of the respective demodulation modules. That is, the AGC circuits 15 and 16 have their amplification gains raised, unlike the composition circuit 43, when the input signal is lower. Even if, therefore, there is a difference between the input signals of both the demodulation modules, control is made by the AGC circuits to attain a given level. It is, therefore, not possible to differentiate between the received signal and the AGC-amplified noise upon mere calculation on the ratio of the signal powers.

[0017] If the signals of the respective demodulation modules are independently AGC-controlled on the OFDM receiver unit using the diversity configuration, if the mere weights proportional to the powers of the received signals are used, the normal operation of the diversity is restricted only to the case where the reception states of the respective demodulation modules are to the same extent. Therefore, an OFDM receiver unit is desired which can perform faultless diversity operation even if the reception states of the respective demodulation modules differ.

[0018] According to an aspect of the present invention, there is provided an OFDM receiver unit characterized by comprising a first demodulation module (DMM1) configured to receive an OFDM signal and demodulate data from the OFDM signal, the output signal thereof being controlled to a given level by a first automatic gain control circuit (15); a second demodulation module (DMM2) configured to receive the OFDM signal and demodulate data from the OFDM signal, the output signal thereof being controlled to a given level by a second automatic gain control circuit (16); a first detection circuit (29) configured to detect a quality of the data demodulated by the first demodulation module; a second detection circuit (31) configured to detect a quality of data demodulated by the second demodulation module; a decision circuit (33) configured to decide the qualities of the received signals in accordance with detection signals supplied from the first and second detection circuits; and an output circuit (34) supplied with data from the first and second demodulation modules and decision signal from the decision circuit, the output circuit (34) being configured to output the data supplied from the first and second demodulation modules in accordance with the decision circuit (34) and the data coming from the output circuit (34) having a better quality.

[0019] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0020] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing one form of a conventional OFDM receiver unit using a diversity configuration;

FIG. 2 is a block diagram showing one practical form of a composition circuit shown in FIG. 1;

FIG. 3 is a block diagram showing an OFDM receiver unit according to a first embodiment of the present invention;

FIG. 4 is a block diagram according to one practical form of a composition circuit shown in FIG. 3;

FIG. 5 is a block diagram showing one form of an S/N detection circuit shown in FIG. 3;

FIG. 6 is a block diagram showing one practical form of a decision circuit shown in FIG. 3;

FIG. 7 is a block circuit showing an OFDM receiver unit according to a second embodiment of the present invention;

FIG. 8 is a block diagram showing one form of a selection circuit shown in FIG. 7;

FIG. 9 is a block diagram showing an OFDM receiver unit according to a third embodiment of the present invention;

FIG. 10 is a block diagram showing one form of a decision circuit shown in FIG. 9;

FIG. 11 is a block diagram showing an OFDM receiver according to a fourth embodiment of the present invention, one form of a decision circuit thereof being shown;

FIG. 12 is a block diagram showing an OFDM receiver unit according to a fifth embodiment of the present invention;

FIG. 13 is a block diagram showing one practical form of a decision circuit shown in FIG. 12;

FIG. 14 is a block diagram showing an OFDM receiver unit according to a sixth embodiment of the present invention; and

FIG. 15 is a block diagram showing an OFDM receiver unit according to a seventh embodiment of the present invention.

[0021] The embodiments of the present invention will be described below with reference to the accompanying drawing.

(First Embodiment)

[0022] FIG. 3 shows a first embodiment of the present invention. The same reference numerals are employed to designate parts or elements corresponding to those shown in FIG. 1 and an explanation will be made below about those different portions only.

[0023] The first embodiment has the function of detecting a reception quality of each demodulation module so as to secure a correct diversity operation even if the reception states of the respective demodulation modules differ.

[0024] That is, in FIG. 3, an S/N detection circuit 29 is connected to the output terminal of an equalization circuit 27 and an S/N detection circuit 31 is connected to an output terminal of the equalization circuit 28. These S/N detection circuits 29 and 31 detect S/N ratioes of signals outputted from the equalization circuits 27 and 28, respectively, and the output signals of the S/N detection circuits 29 and 31 are supplied to a decision circuit 33.

[0025] The decision circuit 33 outputs decision signals lv1 and lv2 for deciding the reception qualities of both demodulation modules DMM1 and DMM2 on the basis of the signals supplied from the S/N detection circuits 29 and 31. These decision signals lv1 and lv2, as well as the signal powers from power detection circuits 30 and 32 and output signals from the equalization circuits 27 and 28, are supplied to a composition circuit 34 as an output circuit.

[0026] FIG. 4 is one form of the composition circuit 34. The composition circuit 34 includes multipliers 341 and 342, ratio calculating section 343, multipliers 344 and 345 and adder 346. The decision signal lv1 from the decision circuit 33 is supplied to the multiplier 341 and the signal power pw1 from the power detection circuit 30 is supplied to the multiplier 341. Further, the decision signal lv2 from the decision circuit 33 is supplied to the multiplier 342 and the signal power pw2 from the power detection circuit 32 is supplied to the multiplier 342. The respective multipliers 341 and 342 add weights, by the decision signals lv1 and lv2, to the signal powers pw1 and pw2 supplied from the power detection circuits 30 and 32. If the reception quality is deteriorated by the weight addition, the signal power value becomes smaller.

[0027] The signal powers pw1' and pw2' weighted by the multipliers 341 and 342 are supplied to a ratio calculating section 343 where proportion values f1 and f2 given below are calculated based on the signal power values pw1' and pw2' thus weighted.

$$f1 = pw1'/(pw1' + pw2')$$

$$f2 = pw2'/(pw1' + pw2')$$

[0028] The proportion value f1 is supplied to one input terminal of the multiplier 344 and the proportion value f2 is supplied to one input terminal of the multiplier 345. A data signal D1 from the equalization circuit 27 in the demodulation module DMM1 is supplied to the other input terminal of the multiplier 344 and a data signal D2 from the equalization circuit 28 in the demodulation module DMM2 is supplied to the other input terminal of the multiplier 345. In the multipliers 344 and 345, the respective data signals D1, D2 are weighted by the proportion values f1 and f2.

[0029] The output signals of the multipliers 344 and 345 are supplied to the adder 346 where these signals are added together. A data signal from the respective demodulation modules is composed in a series of processing. A resultant composite signal is supplied to an error correction circuit 35.

[0030] In FIG. 3, the decision signals lv1 and lv2 from the decision circuit 33 are provided as reception level signals 1 and 2 to the user.

[0031] FIG. 5 shows one form of the S/N detection circuit 29. The S/N detection circuit 31 has the same arrangement as that of the S/N detection circuit 29 and any further explanation of it is, therefore, omitted.

[0032] The S/N detection circuit 29 comprises a multiplexer 291, a difference detection circuit 292, a multiplier 293, an addition circuit 294 and a register 295. The multiplexer 291 selects either an I axis signal or a Q-axis signal from the equalization circuits 27 in accordance with a select signal SEL. The output signal of the multiplexer 291 is supplied to the difference detection circuit 292. The difference detection circuit 292 detects a difference from a reference mapping position nearest to an input signal to the input signal. A signal detected by the difference detection circuit 292 is supplied to the multiplier 293 where it is squared. The output signal of the multiplier 293 is sequentially supplied to the addition circuit 294 and then to the register 295 and, by doing

so, a cumulative add value is detected by the addition circuit 294 and register 295. Therefore, the squared sum of the differences is retained in the register 295. It is to be noted that the register 295 is initialized (cleared) by a control signal CTRL at a starting time point of an OFDM symbol and a write-in operation is controlled. The control signal CTRL has its timing set in such a way as to calculate a cumulative add value only with respect to a signal (for example, a pilot signal) in a defined position of an OFDM signal.

[0033] In an ideal transmission path, the reference mapping positions of the I axis signal and Q axis signal outputted from the equalization circuit 27 are made equal. Thus, the difference from the reference mapping position becomes "0" and the cumulative add value retained in the register 295 also becomes "0". However, a signal in a practical transmission path contains various kinds of interference signal components such as noise, multipath and fading and, for this reason, the cumulative add value necessarily never becomes "0", that is, it becomes other than "0". The cumulative add value is considered proportional to the noise level in the signal as well as the magnitudes of various kinds of interference signal components. It is, therefore, possible to evaluate the reception quality by the magnitudes of these numerical values. The cumulative add value is supplied as a detection signal sig1 to the decision circuit 33. In the same way, a detection signal sig2 is supplied from the S/N detection circuit 31 to the decision circuit 33.

[0034] FIG. 6 shows one practical form of the decision circuit 33. This decision circuit 33 has a proportion calculation section 331. The detection signals sig1 and sig2 are supplied from the S/N detection circuits 31 and 32 to the proportion calculation section 331 where proportion values s1 and s2 given below are calculated based on the detection signals sig1 and sig2.

$$s1 = sig1/(sig1 + sig2)$$

$$s2 = sig2/(sig1 + sig2)$$

[0035] As set out above, the detection signals sig1 and sig2 are such that, the smaller the bottom value, the better the reception quality of the demodulation module. On the other hand, the decision signals lv1 and lv2 outputted from the decision circuit 33 are used to weight the signal power. For this reason, the better the reception quality, the greater the value it is necessary to reveal. Thus as a decision signal use is made of a result of calculating the proportion value in the other demodulation module. That is, a result of calculating the proportion value s2 is used as the decision signal 1 and a result of calculating the proportion value s1 as the decision signal 2.

[0036] The decision signals lv1 and lv2 of the decision circuit 33 in the demodulation modules are supplied to the composition circuit 34 and used to weight the pilot signal powers. That is, if the reception quality is equal in the respective demodulation modules, the pilot powers are weighted at the same ratio and, if the reception quality is deteriorated, the weight is so added as to set the pilot power to be smaller in accordance with the ratio of the reception quality. By doing so, any adverse effect resulting from the deteriorated reception quality in the corresponding demodulation module can be eliminated in the subsequent stage of processing and it is possible to perform a correct diversity operation. That is, in the ratio of the weighted pilot signal powers, the value of a better reception quality module becomes dominant. As a result, in the weight addition to the output signals of the equalization circuits 27 and 28, the data of the better reception quality module becomes dominant.

[0037] According to the first embodiment, the S/N detection circuits 29, 31 and decision circuit 33 are provided to detect the quality of the received signal in the respective demodulation modules DMM1 and DMM2 and, by deciding the output signals of the S/N detection circuits 29, 31 by means of the decision circuit 33, the reception qualities of the demodulation modules DMM1 and DMM2 are determined and the weight is added by the decision circuit 34 to the received signal in accordance with a result of decision. It is, therefore, possible to eliminate any adverse effect resulting from a deteriorated quality demodulation module and, thereby, perform a correct diversity operation.

[0038] Further, the decision signals lv1 and lv2 are provided as reception level signals 1 and 2 to the user. By doing so, it is possible for the user to recognize any deteriorated reception quality demodulation branch system (demodulation module) and it is, therefore, possible to readily perform a reception quality improving operation in branched units by, for example, adjusting the antenna in the branched unit.

(Second Embodiment)

[0039] An explanation will be made below about the second embodiment of the present embodiment. In FIG. 7, the same reference numerals are employed to designate parts or elements corresponding to those shown in FIG. 3 and an explanation is restricted to those different portions only.

[0040] In the second embodiment, a selection circuit 36 as an output circuit shown in FIG. 7 is provided in place of the composition circuit 34 shown in FIG. 3. This selection circuit 36 adds weights to signal powers pw1 and pw2 from power detection circuits 30 and 32 by decision signals lv1 and lv2 supplied from a decision circuit 33. The selection circuit selects, from data signals D1 and D2 outputted from equalization circuits 27 and 28, one having a greater pilot power by the weighted signal power and delivers it as an output.

[0041] FIG. 8 shows one practical form of the selection circuit 36. The selection circuit 36 comprises multi-

pliers 361, 362, a comparator 363 and multiplier 364. The decision signal lv1 from the decision circuit 33 and signal power pw1 from the power detection circuit 30 are supplied to the multiplier 361. The decision signal lv2 from the decision circuit 33 and signal power pw2 from the power detection circuit 32 are supplied to the multiplier 362. The multipliers 361 and 362 add weights by the decision signals lv1 and lv2 to the signal powers pw1 and pw2 supplied from the power detection circuits 30 and 32, respectively. If, by doing so, the reception quality is equal in the respective demodulation module, the pilot power is weighted at the same ratio. If, on the other hand, the reception quality is deteriorated, the weight is added to set the pilot power lower, in accordance with the reception quality ratio.

[0042] The weighted signal powers pw1' and pw2' outputted from the multipliers 361 and 362 are supplied to the comparator 363 where a comparison is made between the magnitudes of these weighted signal powers. The output signal of the comparator 363 is supplied to the multiplexer 364. The data signals D1 and D2 from the equalization circuits 27 and 28 are supplied to the input terminals of the multiplexer 364 where one of the data signals D1 and D2 is selected by an output signal of the comparator 363. That is, the multiplexer 364 selects the greater pilot signal powers in accordance with the output signal of the comparator 363. That is, the multiplexer 364 can positively select a demodulation module of a better reception quality.

[0043] According to the second embodiment above, the S/N detection circuits 29 and 31 are provided to detect the quality of the received signal in the respective demodulation modules DMM1 and DMM2 and the reception quality in the demodulation modules DDM1 and DDM2 is decided by the output signals of these S/N detection circuits 29 and 31. The selection circuit 36 adds the weight to the received signal by a result of decision and selects the greater pilot signal power, by the weighed signal power, from the data signals outputted from the equalization circuits 27 and 28 and delivers it as an output. It is, therefore, possible to eliminate any adverse effect resulting from the demodulation module of a deteriorated reception quality and to perform a correct diversity operation.

(Third Embodiment)

[0044] An explanation will be made below about the third embodiment of the present invention.

[0045] FIG. 9 shows a third embodiment of the present invention. In FIG. 9, the same reference numerals are employed to designate parts or elements corresponding to those shown in FIG. 3 and an explanation will be made below about different portions only.

[0046] A decision circuit 37 shown in the third embodiment is different from the decision circuit 33 of the first embodiment in terms of their internal arrangement. Further, the input terminals of inverter circuits 41 and 42 are connected to the output terminals of the decision circuit 37, respectively. A branch warning signal 1 is outputted from the output terminal of the inverter circuit 41 and a branch warning signal 2 is outputted from the output terminal of the inverter 42.

[0047] FIG. 10 shows an example of the decision circuit 37. This decision circuit 37 comprises registers 371, 372, comparators 373, 374, a NOR circuit 375, and OR circuits 376, 377. The registers 371 and 372 retain an upper limit value and lower limit value of a detection signal. These upper and lower limit values can be properly set externally.

[0048] The comparators 373 and 374 make a comparison as to whether the detection signals 1 and 2 fall within the lower limit value and upper limit value. That is, the comparator 373 compares a detection signal sig1 which is supplied from the S/N detection circuit 29 to the upper and lower limit values from the registers 371 and 372. The comparator 374 compares a detection signal sig2 which is supplied from the S/N detection circuit 31 to the lower and upper limit values which are supplied from the registers 371 and 372. The comparators 373 and 374 output a signal "1" when the detection signal sig1 or sig2 falls within a range between the lower limit value and the upper limit value and output a signal "0" when the detection signal 1 or 2 fall outside the range between the lower limit value and the upper limit value.

[0049] The output signals of the comparators 373 and 374 are supplied to the input terminals of the NOR circuit 375 and to the corresponding input terminals of OR circuits 376 and 377. The output of the NOR circuit 375 is connected to the remaining corresponding input terminals of the OR circuits 376 and 377. Decision signals lv1 and lv2 are outputted from the output terminals of the OR circuits 376 and 377, respectively.

[0050] Here, if the output signals of the comparators 373 and 374 are both "0", both the decision signals lv1 and lv2 are caused to be set to "1" by the NOR circuit 375 and OR circuits 376 and 377.

[0051] As set out above, the decision signals lv1 and lv2 of the demodulation modules which are outputted from the decision circuit 37 are supplied to a composition circuit 34 and used for the weight addition calculation of the pilot signal powers pw1 and pw2 outputted from power detection circuits 30 and 32. That is, if the reception quality in the respective demodulation module falls within a set value, the pilot signal power value itself is supplied by the weight addition calculation to a subsequent stage of processing. If, on the other hand, the reception quality falls outside the set value, then the pilot signal power value is supplied by the weight addition calculation as "0" to a subsequent stage of processing. By doing so, an adverse effect resulting from the demodulation module of a deteriorated reception quality can be eliminated in the subsequent stage of processing and it is possible to perform a correct diversity operation.

[0052] That is, the calculation of a proportion value by the weighted pilot signal power is only made in the mod-

ule of the better reception quality. As a result, the weight addition to the data signals D1, D2 from the equalization circuits 27, 28 is made only to the data signal in the module of the better reception quality.

[0053] According to the third embodiment, the S/N detection circuits 29, 31 are provided for detecting the quality of a received signal in the respective demodulation modules DMM1, DMM2. The decision circuit 37 decides whether the output signals of the S/N detection circuits 29, 31 fall within or outside of a set value range and delivers binary signals as decision signals Iv1, Iv2. Upon receipt of the decision signals Iv1, Iv2 as binary values from the decision circuit 37 the composition circuit 34 allows a weight addition to be made to a better quality reception signal in the demodulation modules DMM1, DMM2. It is therefore, possible to eliminate any adverse effect resulting from the demodulation module of a deteriorated reception quality and to perform a correct diversity operation.

[0054] Further, the decision signals Iv1, Iv2 outputted as binary signals from the decision circuit 37 are delivered as branch warning signals 1, 2 through the inverters 41, 42. For this reason, it is possible for the user to recognize the demodulation module of a deteriorated reception quality with the use of the branch warning signals 1, 2. It is possible to perform a reception quality improving operation by adjusting an antenna, etc., in the modules.

(Fourth Embodiment)

[0055] An explanation will be made below about the fourth embodiment of the present invention. FIG. 11 shows the fourth embodiment and a variant of the decision circuit 37 shown in FIGS. 9 and 10.

[0056] In FIG. 11, a decision circuit 37a comprises a substrator 381, an absolute value circuit 382, a comparator 383, a register 384, an inverter circuit 385, a comparator 386, and OR circuits 387, 388. The substractor 381 calculates a difference value between the detection signals sig1 and sig2 supplied from the S/N detection circuits 29 and 31. The difference value (diff) is supplied to the absolute circuit 382 and comparator 383. The absolute circuit 382 calculates an absolute value (abs-diff) of the difference value and a result of calculation is supplied to the comparator 386. The comparator 386 decides whether or not the absolute value of the difference value is below an upper value (upper) retained in the register 384. In this connection it is to be noted that the upper value retained in the register 384 can be arbitrarily set from an outside. If the absolute value of the difference value is below the upper value, the comparator 386 delivers a "1" signal as being no significant difference in the reception quality of the demodulation modules and sets decision signals Iv1, Iv2 so as to allow both the demodulation modules to be set active.

[0057] On the other hand, the comparator 383 decides whether the difference value (diff) is positive or not and delivers a "1" signal when the difference value (diff) is positive and a "0" signal when the difference value (diff) is negative.

[0058] If the absolute value of the difference value exceeds the upper value, as a result of comparison by the comparator, a signal outputted from the comparator 386 is set to "0". For this reason, the decision signals Iv1, Iv2 outputted from the OR circuits 387, 388 are set depending upon the output signals of the comparator 383 and inverter circuit 385 and it is possible to set the demodulation module of a smaller detection signal value only effective.

[0059] As set out above, the first and second decision signals Iv1 and Iv2 of the demodulation modules which are outputted from the decision circuit 37a are supplied to the composition circuit 34 and used for the weight addition to the pilot signal powers outputted from the power detection circuits 30, 32. That is, if there is no significant difference in reception quality in the respective demodulation modules, a corresponding pilot signal power value itself is fed to a subsequent stage of processing. If, on the other hand, there is a significant difference, a corresponding pilot signal power value in the demodulation module of a deteriorated reception quality is fed as "0" to the subsequent stage of processing. Any adverse effect resulting from the demodulation module of a deteriorated reception quality can be eliminated in the subsequent stage and it is possible to perform a correct diversity operation.

[0060] That is, the proportion value based on the weighted pilot signal power is calculated in the module of a better reception quality only. As a result, the weight addition to the data signals D1, D2 outputted from the equalization circuit 27, 28 is performed relative to the data signal in the better reception quality module only.

[0061] According to the fourth embodiment, it is possible to obtain the same advantage as that of the second embodiment.

(Fifth Embodiment)

[0062] The fifth embodiment of the present invention will be described below.

[0063] FIG. 12 shows a fifth embodiment of the present invention. In FIG. 12, the same reference numerals are employed to designate parts or elements corresponding to those shown in FIG. 3 and an explanation will be made only about the different portions.

[0064] The decision circuit 33 shown in FIG. 3 is replaced by a decision circuit 39 in FIG. 12. That is, input signal levels 1 and 2 coming from AGC circuits 15, 16 are supplied to the decision circuit 39 in FIG. 12. The decision signals Iv1, Iv2 from the decision circuit 39, together with signal powers from power detection circuits 30, 32 and output signals from equalization circuits 27, 28 are supplied to a composition circuit 34.

[0065] In FIG. 12, input signal levels in1, in2 from the AGC circuits 15, 16 mean the field intensities of input

signals fed from antennas 11, 12. In general, the greater the field intensity the greater the input levels in1, in2. And the reception state becomes better. In the fifth embodiment, the reception states of the demodulation modules are decided using the input signal levels in1, in2.

[0066] FIG. 13 shows one practical form of the decision circuit 39. This decision circuit 39 has a proportion calculation section 391. Input signal levels in1, in2 coming from the AGC circuits 15, 16 are supplied to the proportion calculation section 391 where comparison values given below are calculated based on the input signals in1, in2.

$$s1 = in1/(in + in2)$$

$$s2 = in2/(in1 + in2)$$

[0067] As set above, it is shown that the greater the input signal levels in1, in2, the better the reception quality in the demodulation module. Further, the decision signals Iv1, Iv2 from the decision circuit 39 are used to add the weights to the signal powers in the subsequent stage of processing. For this reason, as the reception quality becomes better, it is necessary to reveal the greater value. Therefore, the results s1, s2 of calculating the proportion values of the input signal levels in1, in2 are used directly as the decision signals Iv1, Iv2.

[0068] According to the fifth embodiment above, the decision circuit 39 decides the reception qualities of the demodulation modules DMM1, DMM2 by the input signal levels in1, in2 of these demodulation modules and the composition circuit 34 adds weights to data signals D1, D2 coming from equalization circuits 27, 38 in accordance with the decision signals Iv1, Iv2 supplied from the decision circuit 39. It is, therefore, possible to eliminate any adverse effect resulting from the demodulation module of a deteriorated reception quality and to perform a correct diversity operation.

(Sixth Embodiment)

[0069] An explanation will be made below about the sixth embodiment of the present invention.

[0070] FIG. 14 shows the sixth embodiment of the present invention. In FIG. 14, the same reference numerals are employed to designate parts or elements corresponding to those shown in FIGS. 9 and 10 and an explanation will be made below about different portions only.

[0071] The sixth embodiment is different from the third embodiment in the following respects.

[0072] In FIGS. 9 and 10, the detection signals sig1, sig2 outputted from the S/N detection circuits 29, 31 are supplied to the decision circuit 37, while, in FIG. 14, input signal levels in1 and in2 outputted from AGC circuits 15 and 16 are supplied to a decision circuit 37. That is, the input signal levels in1, in2 from the AGC circuits 15, 16 are supplied to the input terminals of the comparators 373, 374 shown in FIG. 10.

[0073] In FIG. 14, the input signal levels in1, in2 from the AGC circuits 15, 16 are the field intensities of input signals supplied from antennas 11, 12. Generally, the greater the field intensity the better the reception state. That is, in the sixth embodiment, the reception state in the demodulation modules is decided by the input signal level.

[0074] As set out above, decision signals Iv1, Iv2 in the demodulation modules outputted from the decision circuit 37 are supplied to a composition circuit 34. Power detection circuits 30, 32 add weights to pilot signal powers outputted therefrom in accordance with the decision signals Iv1, Iv2. The decision signals Iv1, Iv2 are comprised of binary signals "0", "1". For this reason, the multipliers 341, 342 in the composition circuit shown in FIG. 4 supply a pilot signal power value per se to a subsequent stage of processing if the reception quality in the respective demodulation module falls within a set value and supply a pilot signal power value as "0" to a subsequent stage of processing if the reception quality in the demodulation modules falls outside the set value. Any adverse effect resulting from the demodulation module of a deteriorated reception quality can be eliminated and it is therefore possible to perform a correct diversity operation.

[0075] According to the sixth embodiment above, the decision circuit 37 decides the reception quality in the demodulation modules DMM1, DMM2 based on the input signal levels in1, in2 supplied from the AGC circuits 15, 16 of the demodulation modules DMM1, DMM2 and outputs the decision signals Iv1, Iv2. For this reason, the weight addition calculation can be performed by only a received signal of a better quality in accordance with the decision signals Iv1, Iv2. Therefore, any adverse effect resulting from a demodulation module of a deteriorated reception quality can be eliminated and it is therefore possible to perform a correct diversity operation.

(Seventh Embodiment)

[0076] An explanation will be made below about the seventh embodiment of the present invention.

[0077] FIG. 15 shows the seventh embodiment of the present invention, constituting a variant of the sixth embodiment. In FIG. 15, the same reference numerals are employed to designate parts or elements corresponding to those shown in FIG. 14 and an explanation will be made below about the different portions.

[0078] In FIG. 15, the decision circuit 37 shown in FIG. 14 is replaced by a decision circuit 37a. This decision circuit 37a has the same arrangement as that of the decision circuit 37a shown in FIG. 11 except that different input signals are used.

[0079] That is, input signal levels in1, in2 coming from

AGC circuits 15, 16 are supplied to the input terminals of the decision circuit 37a shown in FIG. 15, that is, to a subtractor 381 shown in FIG. 11. Therefore, the subtractor 381 calculates a difference between these input signal levels in1, in2 and the decision circuit 37a decides a reception quality in demodulation modules DMM1, DMM2 based on the input signal levels in1, in2.

[0080] The decision signals lv1, lv2 outputted from the decision circuit 37a are supplied to a composition circuit 34 and used to add weights to pilot signal powers outputted from the power detection circuits 30, 32. The pilot signal power values per se are supplied to a subsequent stage of processing if there is no significant difference in reception quality in the respective demodulation modules. If, on the other hand, there is any significant difference, the pilot signal power value in the demodulation module of a deteriorated reception quality is sent as "0" in a subsequent stage of processing. By doing so, any adverse effect resulting from the demodulation module of a deteriorated reception quality can be eliminated in the subsequent stage of processing and it is therefore possible to perform a correct diversity operation.

[0081] According to the seventh embodiment, the reception quality in the demodulation modules DMM1, DMM2 is determined by the decision circuit 37a based on the input signal levels of the demodulation modules DMM1, DMM2. For this reason, the weight addition calculation can be done only on the received signal of a better quality based on the decision signals lv1, lv2 supplied from the decision circuit 37a. Therefore, any adverse effect resulting from the demodulation module of a deteriorated reception quality can be eliminated and it is therefore possible to perform a correct diversity operation.

[0082] Although, in the first to seventh embodiments, the demodulation modules have been explained as being of a two-system type, it is possible to adopt a three or more system type.

Claims

1. An OFDM receiver unit **characterized by** comprising:

   a first demodulation module (DMM1) configured to receive an OFDM signal and demodulate data from the OFDM signal, an output signal thereof being controlled to a given level by a first automatic gain control circuit (15);
   a second modulation module (DMM2) configured to receive the OFDM signal and demodulate data from the OFDM signal, an output signal thereof being controlled to a given level by a second automatic gain control circuit (16);
   a first detection circuit (29) configured to detect a quality of the data demodulated by the first demodulating module;
   a second detection circuit (31) configured to detect a quality of the data demodulated by the second demodulation module;
   a decision circuit (33) configured to decide the qualities of received signals in accordance with detection signals supplied from the first and second detection circuits; and
   an output circuit (34) supplied with the data from the first and second demodulation modules and decision signal from the decision circuit, the output circuit (34) being configured to output the data supplied from the first and second demodulation modules in accordance with the decision signal of decision circuit and the data coming from the output circuit (34) having a better quality.

2. An OFDM receiver unit according to claim 1, **characterized in that** the first demodulation module (DDM1) comprises:

   a first Fourier transformation circuit (23) configured to demodulate data of each subcarrier of the OFDM signal;
   a first pilot signal interpolation circuit (25) configured to interpolate a pilot signal contained in a signal which is supplied from the first Fourier transformation circuit (23);
   a first equalization circuit (27) configured to generate a first subcarrier signal in accordance with the signal from the first Fourier transformation circuit (23) and pilot signal supplied from the first pilot signal interpolation circuit (25); and
   a first power detection circuit (30) configured to detect the power of the first pilot signal supplied from the first pilot signal interpolation circuit (25).

3. An OFDM receiver unit according to claim 1, **characterized in that** the second demodulation module (DMM2) comprises:

   a second Fourier transformation circuit (24) configured to demodulate data in each subcarrier of the OFDM signal;
   a second pilot signal interpolation circuit (26) configured to interpolate a pilot signal contained in a signal supplied from the second Fourier transformation circuit (24);
   a second equalization circuit (28) configured to generate a third subcarrier signal in accordance with the signal supplied from the second Fourier transformation circuit (24) and pilot signal supplied from the second pilot signal interpolation circuit (26); and
   a second power detection circuit (32) config-

ured to detect the power of a second pilot signal supplied from the second pilot signal interpolation circuit (26).

4. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (33) has a proportion calculation section (331) supplied with first and second detection signals (sig1, sig2) outputted from the first and second detection circuits (29, 31), the ratio calculation section (331) being configured to make proportion calculation on the first and second detection signals and generate a first decision signal (s1) corresponding to the second detection signal and a second decision signal (s2) corresponding to the first detection signal and output the first decision signal in a way to correspond to the first demodulation module (DMM1) and the second decision signal in a way to correspond to the second demodulation module (DMM2).

5. An OFDM receiver unit according to claim 2 or 3, **characterized in that** the first detection circuit (29) is configured to detect a signal to noise ratio of a subcarrier signal outputted from the first equalization circuit (27) and the second detection circuit (31) is configured to detect a signal to noise ratio of a subcarrier signal outputted from the second equalization circuit (28).

6. An OFDM receiver unit according to claim 5, **characterized in that** the first and second detection circuits (29, 31) each include a difference detection circuit (292) configured to detect a difference from a reference mapping position to an input signal and an adder (294, 295) configured to cumulatively add an output signal of the difference detection circuit.

7. An OFDM receiver unit according to claim 2, **characterized in that** the output circuit (34) comprises:

a first weight addition circuit (341) supplied with an output signal (pw1) of the first power detection circuit (30) and first decision signal (lv1) outputted from the decision circuit (33), the first weight addition circuit (341) being configured to add a weight to the output signal (pw1) of the first power detection circuit (30) in accordance with the first decision signal (lv1);
a second weight addition circuit (342) supplied with an output signal of a second power detection circuit (32) and second decision signal (lv2) outputted from the decision circuit (33), the second weight addition circuit (32) being configured to add a weight to the output signal of the second power detection circuit (32) in accordance with the second decision signal (lv2);
a proportion calculation section (343) supplied with the first and second weight addition circuits (341, 342), the proportion calculation section (343) being configured to perform a proportion calculation on the output signals of the first and second weight addition circuits (341, 342) to generate first and second weight signals (f1, f2);
a third weight addition circuit (344) supplied with an output signal (D1) of the first equalization circuit (27) and first weight signal (f1) outputted from the proportion calculation section (343), the third weight addition circuit (344) being configured to add a weight to the output signal (D1) of the first equalization circuit (27) in accordance with the first weight signal (f1);
a fourth weight addition circuit (345) supplied with an output signal (D2) of the second equalization circuit (28) and second weight signal (f2) outputted from the ratio calculating section (34), the fourth weight addition circuit (345) being configured to add a weight to the output signal of the second equalization circuit (28) in accordance with the second weight signal (f2); and
and an adder (346) supplied with the output signals of the third and fourth weight addition circuits (344, 345) and configured to output a composite signal.

8. An OFDM receiver unit according to claim 2, **characterized in that** the output circuit (36) comprises:

a first weight addition circuit (361) supplied with an output signal (pw1) of the first power detection circuit (30) and first decision signal (lv1) outputted from the decision circuit (33), the first weight addition circuit (361) being configured to add a weight to an output signal of the first power detection circuit (30) by the first decision signal (lv1);
a second weight addition circuit (362) supplied with an output signal (pw2) of the second power detection circuit (32) and a second decision signal (lv2) outputted from the decision circuit (33), the second weight addition circuit (362) being configured to add a weight signal to the output signal (pw2) of the second power detection circuit (32) by the second decision signal (33);
a comparison section (363) supplied with the output signals of the first and second weight addition circuits (361, 362) and configured to compare these output signals with each other; and
a selection circuit (364) supplied with the output signals (D1, D2) of the first and second equalization circuits (27, 28) and result of comparison outputted from the comparison section (363), the selection circuit (364) being configured to select one of the output signals (D1, D2)

of the first and second equalization circuits (27, 28) in accordance with a result of comparison.

9. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (37) comprises:

a first comparator (373) supplied with an output signal (sig1) of the first detection circuit (29) and configured to compare the output signal (sig1) to set values (371, 372) to output a binary signal;
a second comparator (374) supplied with an output signal (sig2) of the second detection circuit (31) and configured to compare the output signal (sig2) to set values (371, 372) to output a binary signal;
a logic circuit (375, 376, 377) supplied with output signals of the first and second comparators (373, 374) and configured to output the first and second decision signals in accordance with the output signals of the first and second comparators (373, 374).

10. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (37a) comprises:

a subtractor (381) supplied with output signals of the first and second detection circuits (29, 31) and configured to calculate a difference between these output signals;
an absolute value circuit (382) supplied with an output signal of the subtractor (381) and configured to calculate an absolute value of this output signal;
a first comparator (386) configured to compare the absolute value outputted from the absolute value circuit (382) to a set value (384) and output a first output signal if the absolute value is greater than the set value;
a second comparator (383) for making a comparison as to whether the output signal of the subtractor (381) is negative or positive; and
a logic circuit (385, 387, 388) supplied with output signals of the first and second comparators (386, 383) and configured to output the first and second decision signals (lv1, lv2) in accordance with an output signal of the second comparator (383) if the first output signal is outputted from the first comparator (386).

11. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (39) is supplied with first and second input signal levels (in1, in2) from the first and second automatic gain control circuits (15, 16) and has a proportion calculation section (391) configured to make a proportion calculation on these first and second input signals and output the first and second decision signals (lvl, lv2) in accordance with a result of calculation.

12. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (37) comprises:

a first comparator (373) supplied with a first input signal level (in1) from the first automatic gain control circuit (15) and configured to compare the first input signal level to a set value and output a binary signal;
a second comparator (374) supplied with a second. input signal outputted from the second automatic gain control circuit (16) and configured to compare the second input signal level (in2) to a set value and output a binary signal; and
a logic circuit (375, 376, 377) supplied with output signals of the first and second comparators and configured to output the first and second decision signals (lv1, lv2) in accordance with the output signals of the first and second comparators (373, 374).

13. An OFDM receiver unit according to claim 1, **characterized in that** the decision circuit (37a) comprises:

a subtractor (381) supplied with input levels (in1, in2) from the first and second automatic gain control circuits (15, 16) and configured to calculate a difference between the first and second input signal levels;
an absolute value circuit (382) supplied with an output signal of the subtractor (381) and configured to calculate an absolute value of the output signal;
a first comparator (386) configured to compare the absolute value from the absolute value circuit (382) to a set value and deliver a first output signal if the absolute value is greater than the set value;
a second comparator (383) configured to make a comparison as to whether the output signal of the subtractor (381) is positive or negative; and
a logic circuit (385, 387, 388) supplied with output signals of the first and second comparators (386, 383) and configured to output the first and second decision signals (lv1, lv2) in accordance with the second comparator (383) if the first output signal is delivered from the first comparator (386).

14. An OFDM receiver unit according to each of claims 1, 8 through 12, **characterized by** further comprising an output circuit (41, 42) connected to the out-

pout terminals of the decision circuit (37, 37a) and configured to output the first and second decision signals (lv1, lv2).

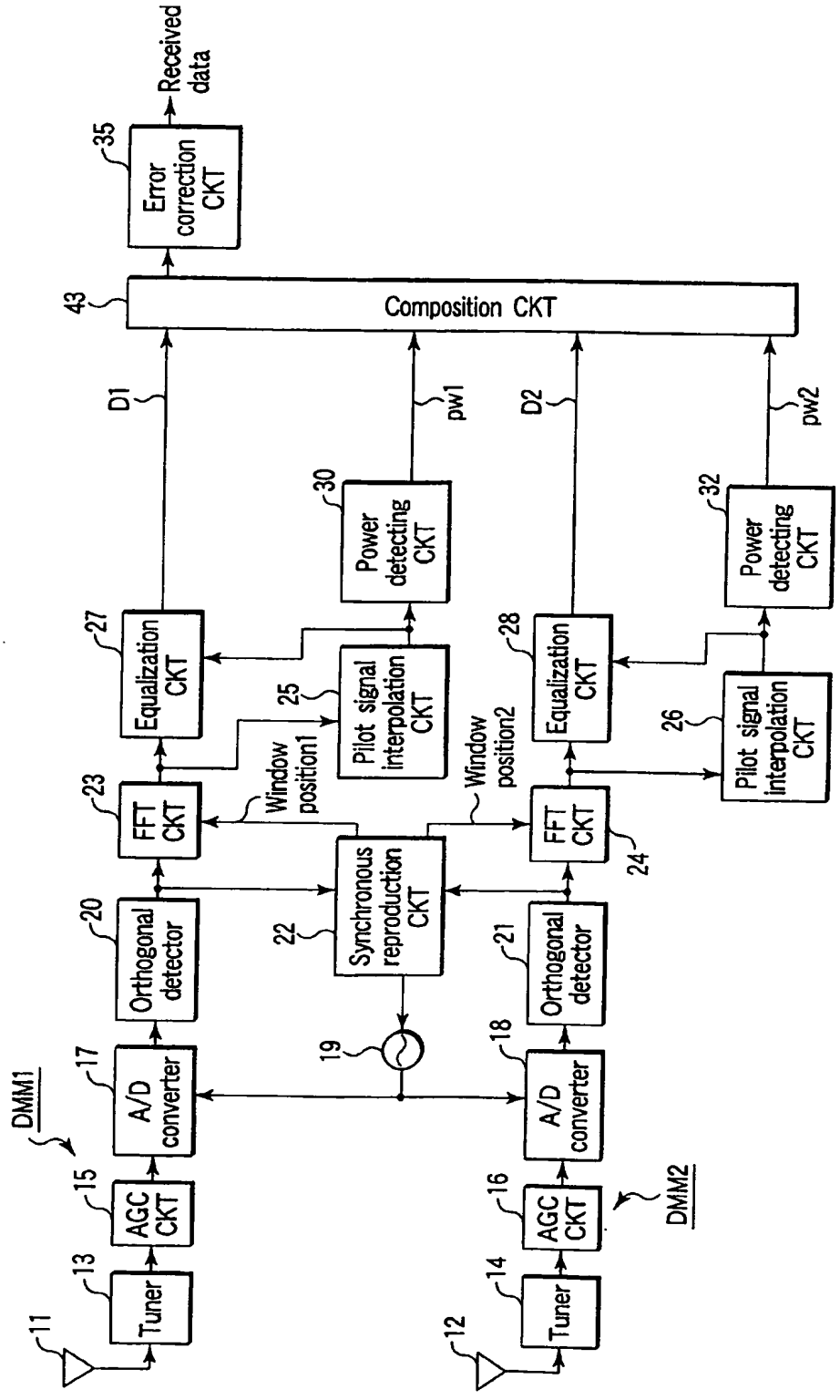
Received data
35
Error correction CKT
43
Composition CKT
D1
pw1
D2
pw2
30
Power detecting CKT
32
Power detecting CKT
27
Equalization CKT
28
Equalization CKT
25
Pilot signal interpolation CKT
26
Pilot signal interpolation CKT
Window position1
Window position2
23
FFT CKT
24
FFT CKT
22
Synchronous reproduction CKT
20
Orthogonal detector
21
Orthogonal detector
19
17
A/D converter
18
A/D converter
DMM1
15
AGC CKT
16
AGC CKT
DMM2
13
Tuner
14
Tuner
11
12

FIG. 1

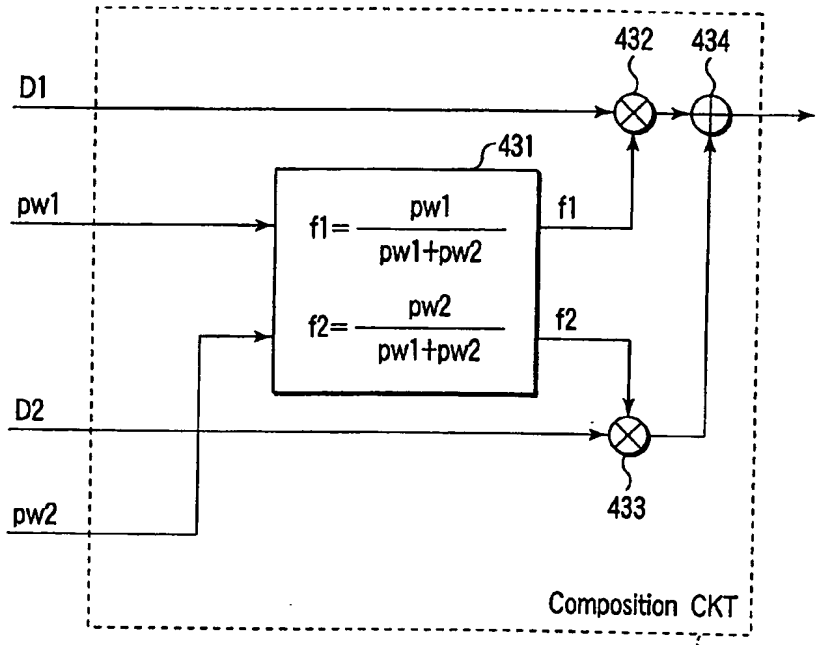
D1
pw1
pw2
D2
431
f1= pw1/(pw1+pw2)
f2= pw2/(pw1+pw2)
f1
f2
432
434
433
Composition CKT
43

FIG. 2

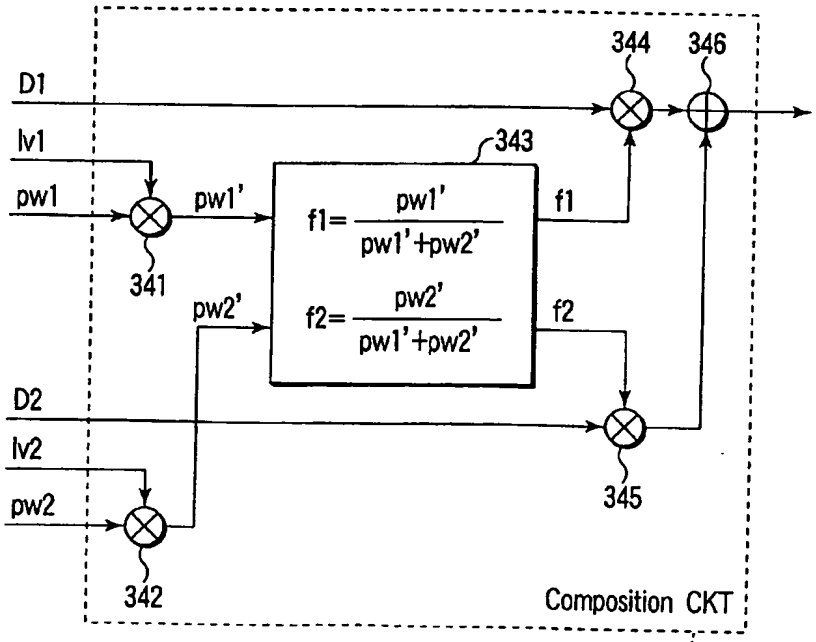
D1
lv1
pw1
pw2'
D2
lv2
pw2
341
342
pw1'
343
f1= pw1'/(pw1'+pw2')
f2= pw2'/(pw1'+pw2')
f1
f2
344
346
345
Composition CKT
34

FIG. 4

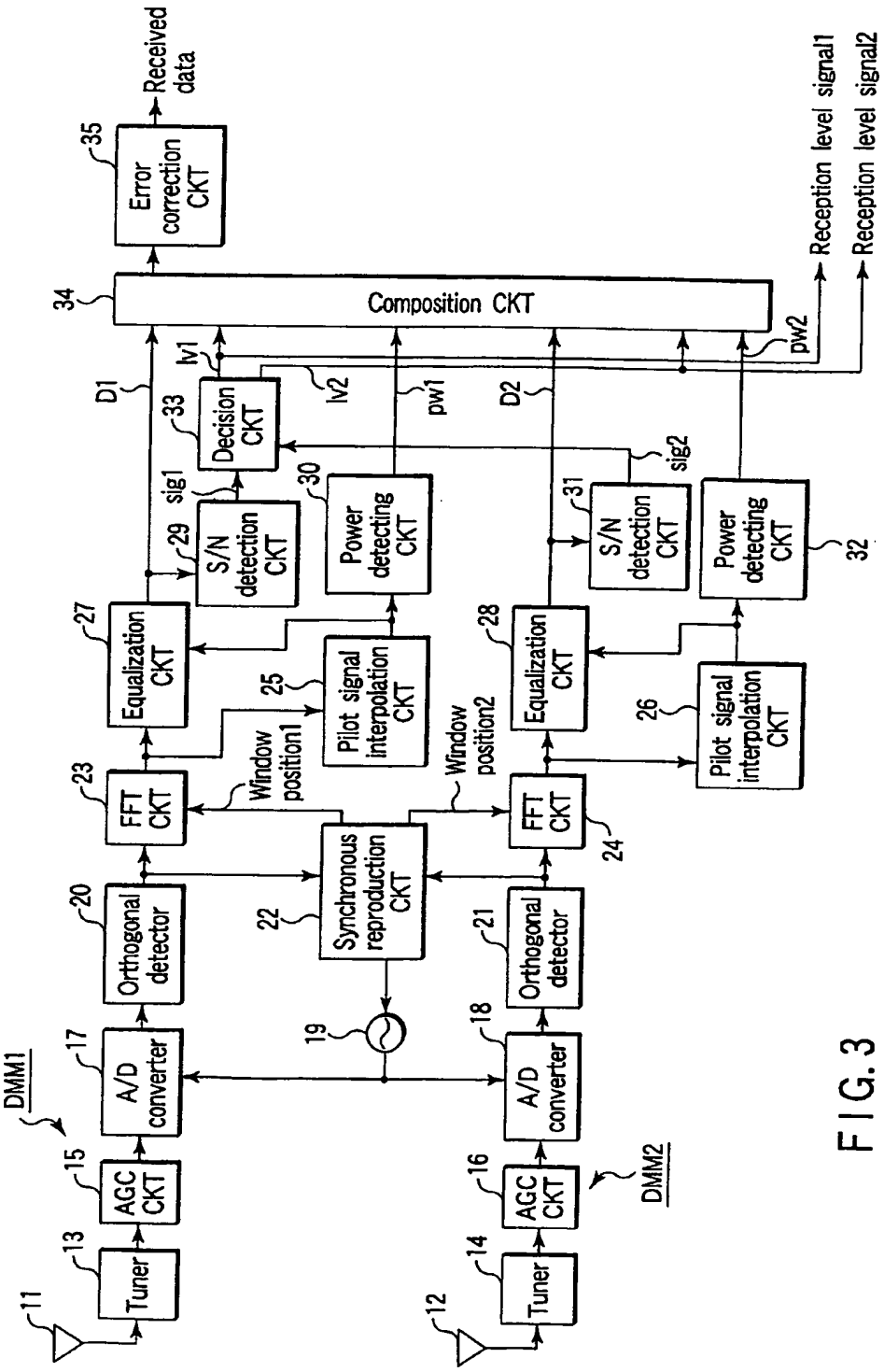
Received data
Error correction CKT
Composition CKT
Reception level signal1
Reception level signal2
Decision CKT
S/N detection CKT
Power detecting CKT
Equalization CKT
Pilot signal interpolation CKT
FFT CKT
Window position1
Window position2
Synchronous reproduction CKT
Orthogonal detector
A/D converter
AGC CKT
Tuner
DMM1
DMM2
D1
D2
lv1
lv2
pw1
pw2
sig1
sig2

FIG. 3

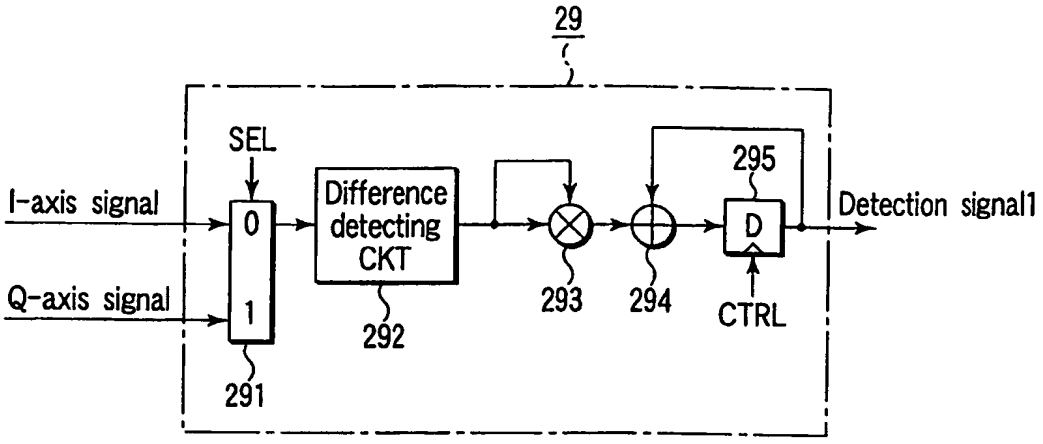
29
SEL
I-axis signal
Q-axis signal
0
1
291
Difference detecting CKT
292
293
294
295
D
CTRL
Detection signal1

FIG. 5

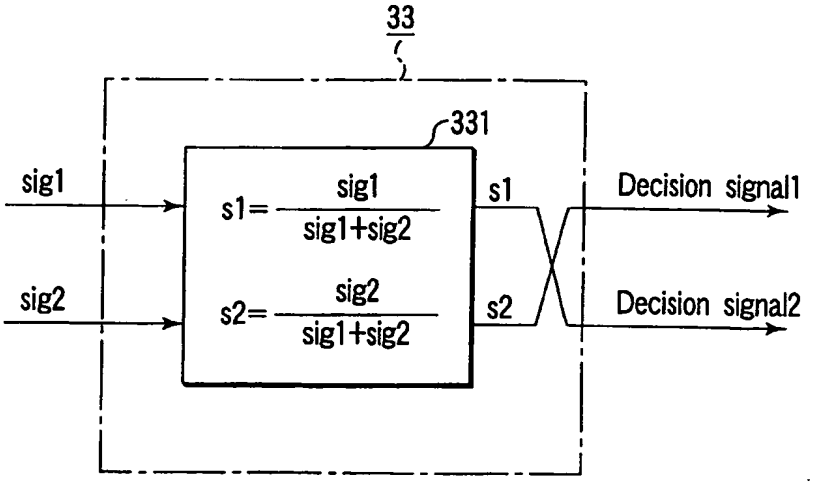
33
331
sig1
sig2
s1= sig1/(sig1+sig2)
s2= sig2/(sig1+sig2)
s1
s2
Decision signal1
Decision signal2

FIG. 6

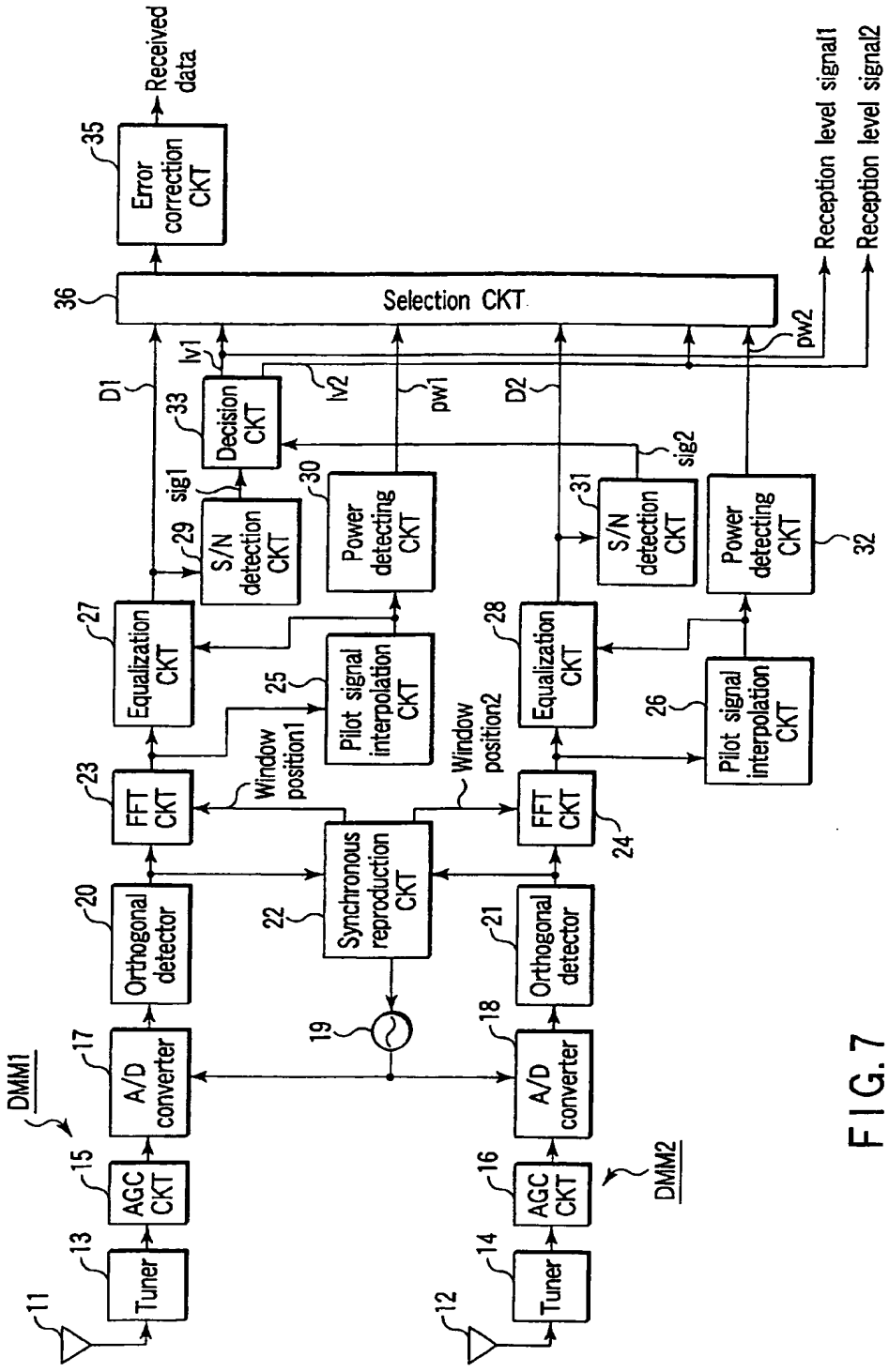
Received data
Error correction CKT
Selection CKT
Reception level signal1
Reception level signal2
Decision CKT
S/N detection CKT
Power detecting CKT
Equalization CKT
Pilot signal interpolation CKT
FFT CKT
Orthogonal detector
Synchronous reproduction CKT
A/D converter
AGC CKT
Tuner
DMM1
DMM2
Window position1
Window position2
D1
D2
lv1
lv2
pw1
pw2
sig1
sig2

FIG. 7

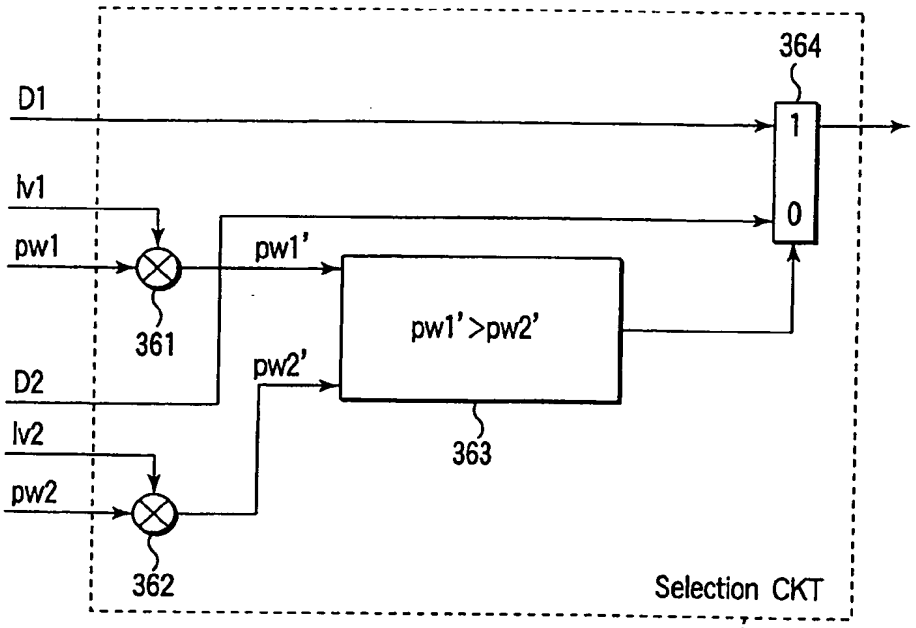
364
D1
1
0
lv1
pw1
pw1'
361
pw1'>pw2'
D2
pw2'
363
lv2
pw2
362
Selection CKT
36

FIG. 8

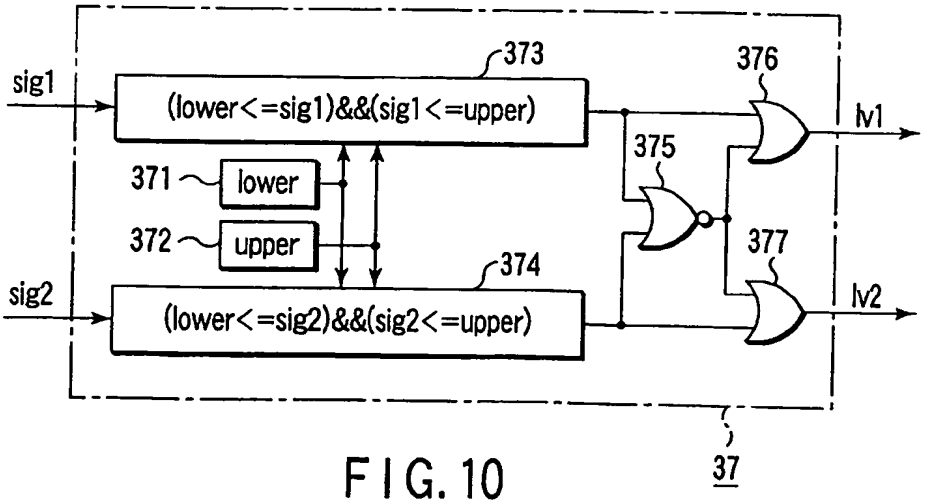
373
376
sig1
(lower<=sig1)&&(sig1<=upper)
lv1
375
371
lower
372
upper
377
374
sig2
(lower<=sig2)&&(sig2<=upper)
lv2
37

FIG. 10

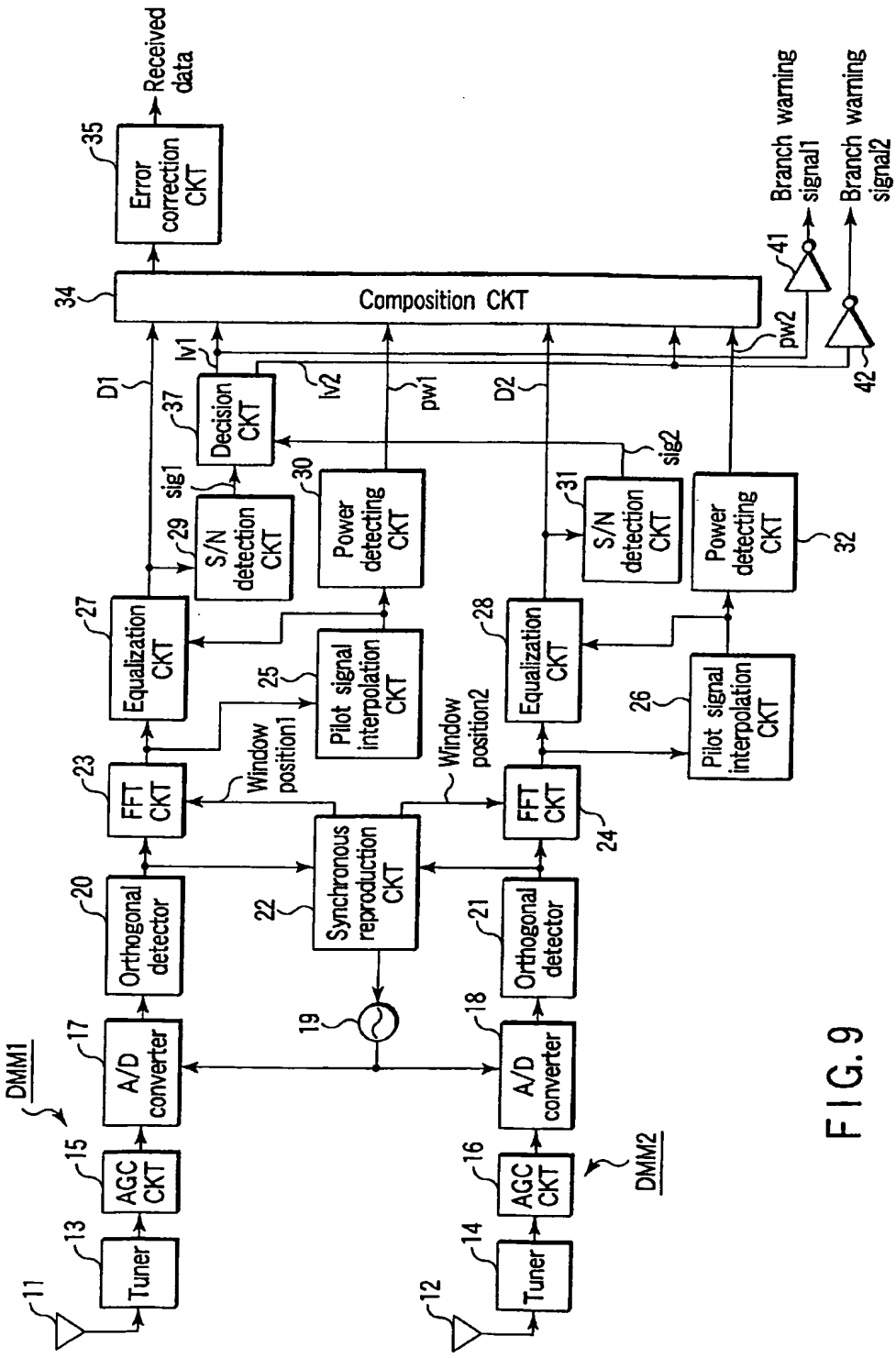
Received data
Error correction CKT
Composition CKT
Branch warning signal1
Branch warning signal2
Decision CKT
S/N detection CKT
Power detecting CKT
Equalization CKT
Pilot signal interpolation CKT
FFT CKT
Synchronous reproduction CKT
Orthogonal detector
A/D converter
AGC CKT
Tuner
DMM1
DMM2
Window position1
Window position2
D1
D2
lv1
lv2
pw1
pw2
sig1
sig2

FIG. 9

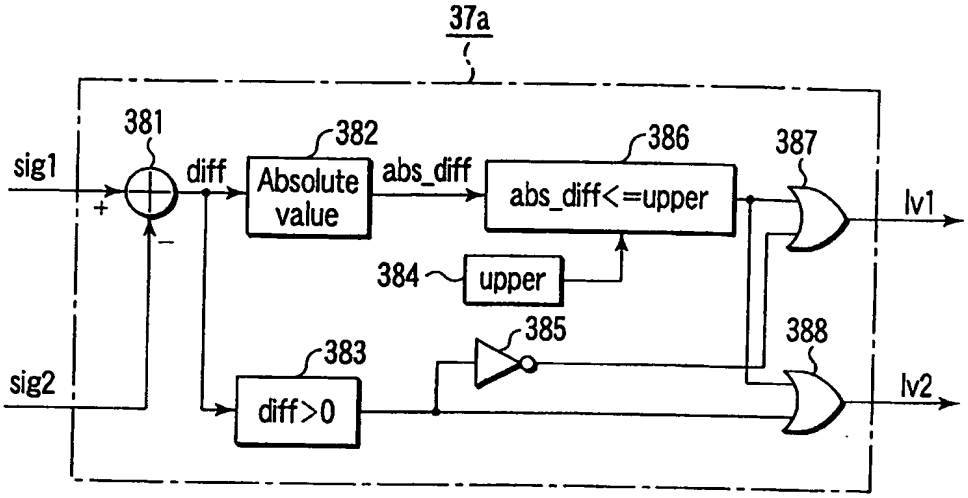
37a
381
382
386
387
sig1
diff
Absolute value
abs_diff
abs_diff<=upper
lv1
+
−
384
upper
385
388
383
sig2
diff>0
lv2

FIG. 11

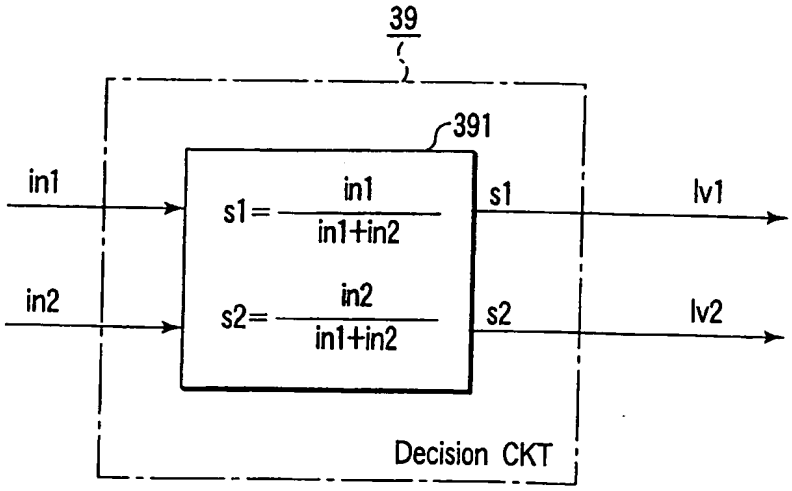
39
391
in1
s1= in1/(in1+in2)
s1
lv1
in2
s2= in2/(in1+in2)
s2
lv2
Decision CKT

FIG. 13

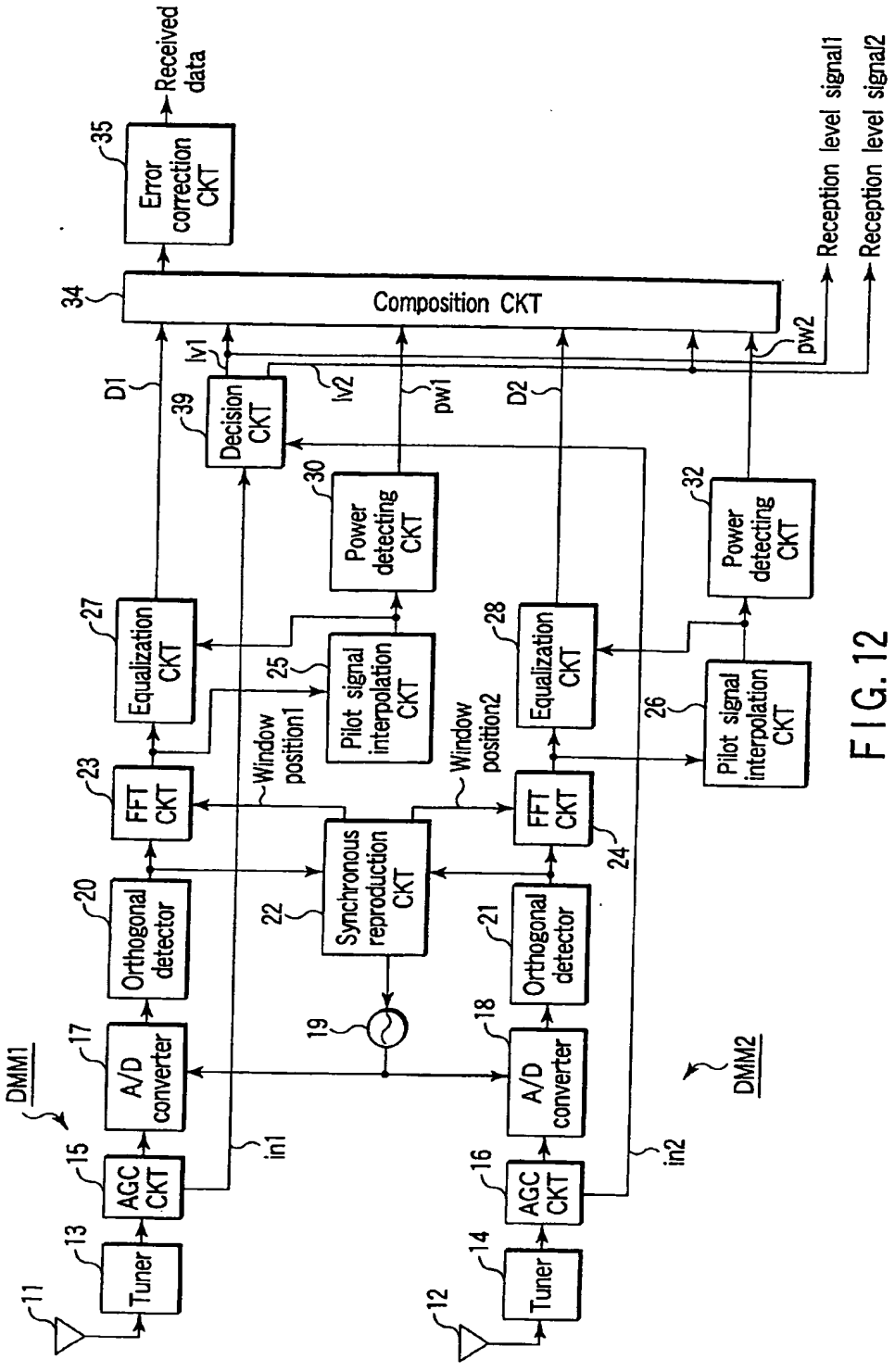
Received data
Error correction CKT
Composition CKT
Reception level signal1
Reception level signal2
Decision CKT
Power detecting CKT
Power detecting CKT
Equalization CKT
Equalization CKT
Pilot signal interpolation CKT
Pilot signal interpolation CKT
FFT CKT
FFT CKT
Window position1
Window position2
Synchronous reproduction CKT
Orthogonal detector
Orthogonal detector
A/D converter
A/D converter
AGC CKT
AGC CKT
Tuner
Tuner
DMM1
DMM2
in1
in2
D1
D2
lv1
lv2
pw1
pw2

FIG. 12

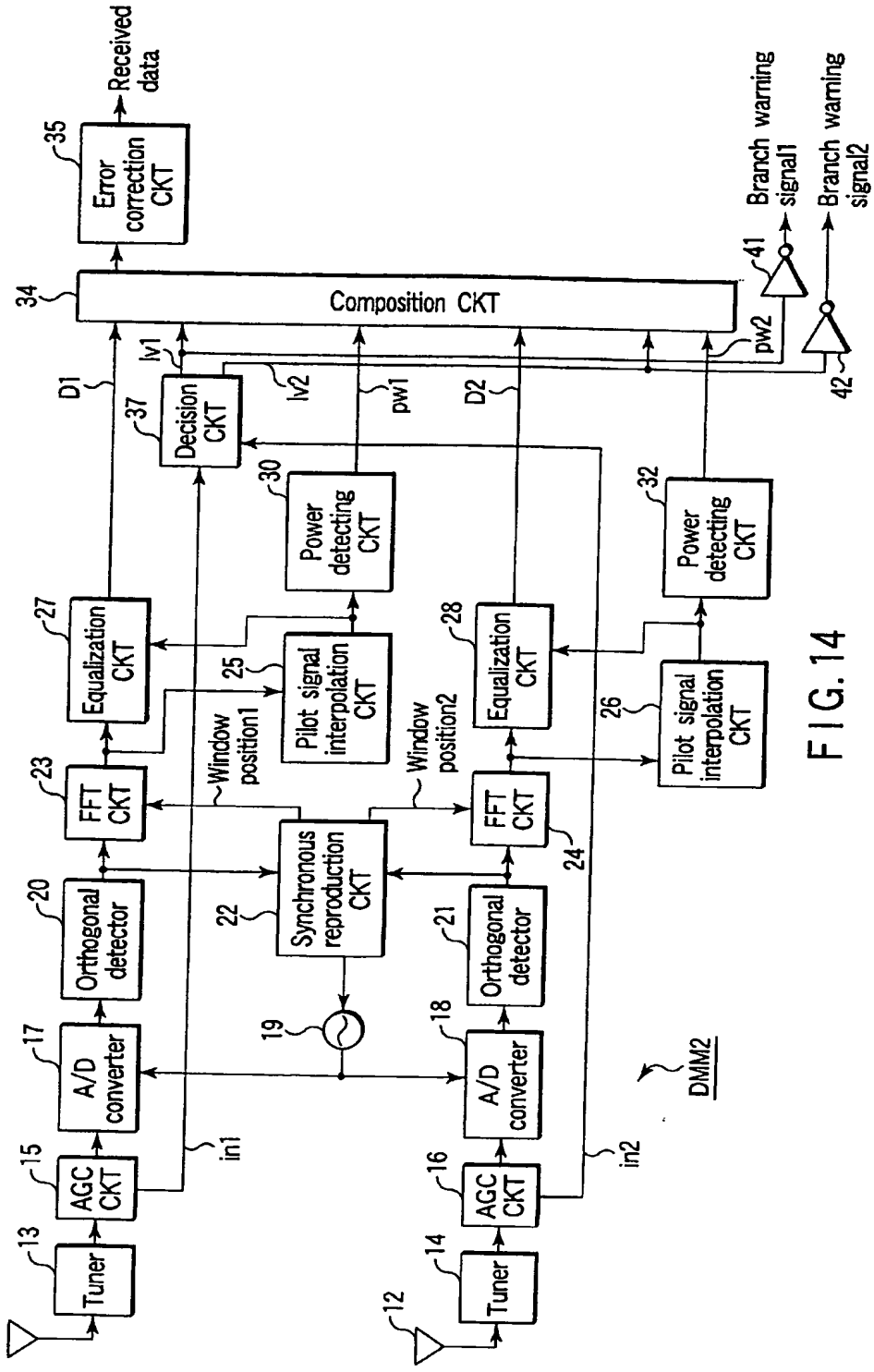
Received data
Error correction CKT
Composition CKT
Branch warning signal1
Branch warning signal2
Decision CKT
Power detecting CKT
Equalization CKT
Pilot signal interpolation CKT
FFT CKT
Window position1
Window position2
Synchronous reproduction CKT
Orthogonal detector
A/D converter
AGC CKT
Tuner
DMM2
in1
in2
D1
D2
lv1
lv2
pw1
pw2

FIG. 14

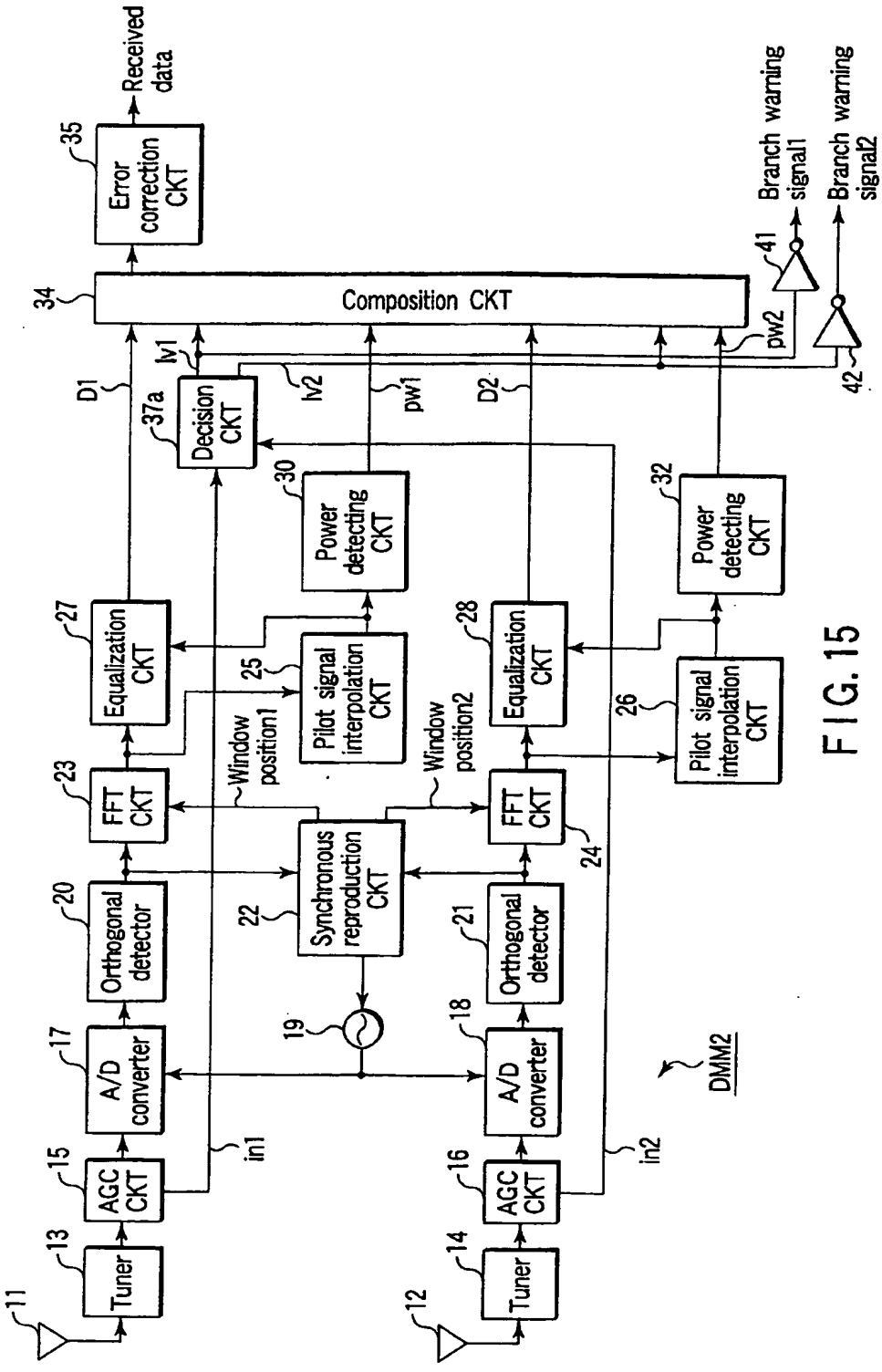
Received data
Error correction CKT
Composition CKT
Branch warning signal1
Branch warning signal2
Decision CKT
Power detecting CKT
Power detecting CKT
Equalization CKT
Equalization CKT
Pilot signal interpolation CKT
Pilot signal interpolation CKT
Window position1
Window position2
FFT CKT
FFT CKT
Synchronous reproduction CKT
Orthogonal detector
Orthogonal detector
A/D converter
A/D converter
AGC CKT
AGC CKT
Tuner
Tuner
in1
in2
DMM2
D1
D2
lv1
lv2
pw1
pw2

FIG. 15

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EUROPEAN SEARCH REPORT

Application Number
EP 02 02 1726

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H04L
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	12 February 2003	Schiffer, A

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